REMARKS

The present Amendment is in response to the Final Office Action having a mailing date of January 22, 2004. Claims 1-21 are pending in the present Application. Claims 1-9 are withdrawn from consideration. Claims 10-21 are rejected. Claims 10 and 16 have been amended for clarification. Consequently, claims 10-21 remain pending in the present application.

Claim Rejections – 35 USC § 102

The Examiner states,

3. Claims 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (6,008,127).

Regarding claim 10, Yamada, figures 1-38, (figures 33, 35, 36, 37, col. 8, lines 52-67, col. 9, lines 1-67), disclose a semiconductor device comprising: a semiconductor substrate 201 including a plurality of device structures (see figure 35) thereon; and an interconnect 235 on the semiconductor substrate, the interconnect comprising at least one slot 235 (see figure 33) provided in the semiconductor substrate and at least one metal 235 (aluminum) within the slot, wherein the at least one slot is oxidized everywhere (see col. 8, lines 52-67) except at the bottom of the slot where the interconnect forms a ground 225 (see col. 9, lines 58-65(. Regarding to claims 11-15, see Yamada, col. 1-14, lines 1-67.

Regarding claim 16, Yamada, figures 1-38, (figures 33, 35, 36, 37, col. 8, lines 52-67, col. 9, lines 1-67), disclose a high voltage interconnect on a semiconductor device comprising: at least one slot 235 provided in the semiconductor substrate 201; and at least one metal 235 (aluminum) within the slot, wherein the at least one slot is oxidized (col. 8, lines 52-67) everywhere except at the bottom of the slot, and the interconnect forms a very low resistance ground trap 225 (see col. 5, lines 61-67, col. 9, lines 15-22, lines 58-65).

Regarding claims 17-21, see Yamada, col. 1-14, lines 1-67.

Applicant traverses this rejection. Applicant has amended claim 10 to clarify the present invention. The present invention as recited in claim 10 provides for a high voltage semiconductor device which includes a seminconductor substrate and an interconnect. The interconnect includes a slot in the substrate and at least one metal within the slot. The metal is of

sufficient thickness to carry a high current. The Yamada ('127) neither teaches nor suggests such a device.

Yamada is directed to a process for fabricating a semiconductor device using an etching stopper film which does not increase the number of photo-etching steps and does not cause a deterioration in device characteristics. It is directed to a conventional semiconductor device and is not concerned with and is not directed toward a high voltage or high power semiconductor device. Furthermore, there is no teaching or suggestion that the metal within the contact holes of Yamada are of sufficient thickness to carry a high current as recited in claim 10. Accordingly, claim 10 is allowable over the cited reference. Furthermore, claims 11-15 are also allowable and they depend from an allowable base claim.

Regarding claim 16, Yamada, figures 1-38, (figures 33, 35, 36, 37, col. 8, lines 52-67, col. 9, lines 1-67), disclose a high voltage interconnect on a semiconductor device comprising: at least one slot 235 provided in the semiconductor substrate 201; and at least one metal 235 (aluminum) within the slot, wherein the at least one slot is oxidized (col. 8, lines 52-67) everywhere except at the bottom of the slot, and the interconnect forms a very low resistance ground trap 225 (see col. 5, lines 61-67, col. 9, lines 15-22, lines 58-65).

Regarding claims 17-21, see Yamada, col. 1-14, lines 1-67.

Applicant traverses this rejection. Applicant has amended claim 16 to clarify the present invention. The present invention as recited in claim 16 provides for a high voltage on a semiconductor substrate. The interconnect includes a slot in the substrate and at least one metal within the slot. The metal is of sufficient thickness to carry a high current. The Yamada ('127) neither teaches nor suggests such a device.

Yamada is directed to a process for fabricating a semiconductor device using an etching stopper film which does not increase the number of photo-etching steps and does not cause a deterioration in device characteristics. It is directed to a conventional semiconductor device and is not concerned with and is not directed toward a high voltage interconnect. Furthermore, there

is no teaching or suggestion that the metal within the contact holes of Yamada are of sufficient thickness to carry a high current as recited in claim 16. Accordingly, claim 16 is allowable over the cited reference. Furthermore, claims 17-21 are allowable since they depend from an allowable base claim.

Conclusion

Therefore, for the above identified reasons, the present invention as recited in independent claims 10 and 16 is neither taught nor suggested by the cited references. Applicant further submits that claims 11-15 and 17-21 are also allowable because they depend on the above allowable base claims.

In view of the foregoing, Applicant submits that claims 10-21 are patentable over the cited reference.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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